CLAIMS:

1. A differential amplifier circuit for regenerating complementary digital signals, which circuit includes a differential pair of transistors (T5, T6) whose inputs (1b, 1a) receive complementary digital signals and whose outputs (OUT, OUTB) deliver regenerated complementary signals, characterized in that it comprises means for reducing the switching time and for increasing the amplitude of the voltage swing between the high and low logic levels of the transistors of the differential pair, which means comprise a pair of push-pull amplifiers (12b, 12a) whose inputs receive the complementary input signals to be regenerated and whose outputs (13b, 13a) deliver, under a low impedance and during the switching, brief and intense current pulses of said complementary input signals of increased amplitude in order to apply these pulses to the inputs of said differential pair of transistors (T5, T6).

2. A circuit as claimed in claim 1, in which the differential pair of transistors (T5, T6) includes a first transistor (T5) and a second transistor (T6), the first transistor (T5) of the pair having a first input (1a) for control and a first electrode (8a) and a second electrode (9a), the second transistor (T6) of the pair having a second input (1b) for control and a first electrode (8b) and a second electrode (9b), the differential pair of push-pull amplifiers (12a, 12b), connected upstream from the differential pair (T5, T6), comprising a first push-pull amplifier (12a) and a second push-pull amplifier (12b), having a first and a second low input (Lb, L), respectively, coupled to a source of the complementary input signal and to a source of the input signal, respectively, a first and a second high input (H, Hb) coupled to a source of the input signal and to a source for the complementary input signal, respectively, a first and a second output (13a, 13b), the first and second outputs (13a, 13b) of the pair of push-pull amplifiers (12a, 12b) being coupled to the first and the second control inputs (1a, 1b) of the first and second transistors (T5, T6) of the differential pair, respectively.

3. A circuit as claimed in one of the claims 1 or 2, in which each amplifier of the pair of push-pull amplifiers (12a, 12b) comprises two transistors (T1, T3 and T2, T4, respectively), each of which comprises a control input (L, Hb, Lb, H), said control inputs

forming the first and second low inputs (L, Lb) and the first and second high inputs (Hb, H) of the pair of push-pull amplifiers (12a, 12b).

4. A circuit as claimed in claim 3, characterized in that the transistors (T5, T6) of the differential pair and the transistors (T1, T2, T3, T4), together forming the pair of push-pull amplifiers (12a, 12b), are field effect transistors whose first and second electrodes (15a, 15b; 17a, 17b) are the sources and the drains, the control inputs being the gates (Lb, L, H, Hb) of the transistors (T1, T2, T3, T4), the drains (17a, 17b) of the high transistors (T3, T4) of each of the push-pull amplifiers (12a, 12b) of the pair of push-pull amplifiers being coupled to a first drain bias source (Vdd1), the drains (8a, 8b) of the transistors (T5, T6) of the differential pair being coupled to a second drain bias source (Vdd2), the sources (15a, 15b) of the low transistors (T1, T2) of each of the push-pull amplifiers (12a, 12b) of the pair of push-pull amplifiers being coupled to a first source voltage source and the sources (9a, 9b) of each of the transistors (T5, T6) of the differential pair being coupled to a second source bias source.

5. A circuit as claimed in claim 4, in which each of the first and second source biases is formed by a current generator (11, 14) or an impedance connected to a voltage source (Vss1, Vss2), respectively.

6. A circuit as claimed in one of the claims 1 to 5, which circuit also comprises, connected upstream from the pair of push-pull amplifiers (12a, 12b), an adaptation circuit (30) for lowering the impedance which delivers, on the basis of the input signal and a complementary signal which is the complement of said input signal, complementary low and high signals which feed the low and high inputs (Lb, L, H, Hb) of the pair of push-pull amplifiers (12a, 12b).

7. A circuit as claimed in claim 6, in which the adaptation circuit (30) includes a follower pair of transistors (T7, T8), each of which has a control input (18a, 18b) and electrodes (19a, 23a, 19b, 23b), one of the control inputs (18a, 18b) of the transistors (T7, T8) of the follower pair receiving the input signal whereas the other control input receives a complementary signal which is the complement of this input signal, respectively, each transistor (T7, T8) of the follower pair being connected in such a manner that one of its electrodes (19a, 19b) carries a follower signal of the signal received on its input (18a, 18b),

which electrode (19a, 19b) is coupled to an input of means (Zs) for changing the level of the signal present on this electrode (19a, 19b), a signal present on an output (21a, 21b) of these means (Zs) being a signal which has the same logic value as the signal present on said input of said means (Zs) but a shifted voltage potential, the low and high inputs (L, Lb, H, Hb) of the pair of push-pull amplifiers (12a, 12b) being formed by the connection nodes present at the input (19a, 19b) and at the output (21a, 21b) of said means (Zs) for changing the level.

8. An emission/transmission circuit for telecommunication, including an amplifier circuit as claimed in one of the preceding claims.

9. An emission module for the transmission/reception of signals via optical fibers, comprising a circuit for reshaping signals and a multiplexing circuit, including an amplifier circuit as claimed in one of the claims 1 to 7.